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(54) **SOLID-STATE IMAGE PICKUP DEVICE**

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the occurrence of a troublesuch as smearsensitivity deteriorationetc.caused by oblique incident light in a solid-state image pickup device.
SOLUTION: The solid-state image pickup device is provided with a plurality of picture elements. In the devicetwo photodiodes 1 and 40 are formed against each picture element. Two light entrance openings 24a and 24b are formed in each light shield film 24 correspondingly to the photodiodes 1 and 40. Oblique light reflecting sections 60-62 which partially reflect the light obliquely made incident to the device through the openings 24a and 24b are partially foamed along the whole circumferences of the openings 24a and 24b at height positions between the photodiodes 1 and 40 and oblique light reflecting films 24.

CLAIMS

[Claim(s)]
[Claim 1]In a solid state camera which has a light-shielding film which it has two or more pixelsand one or more light sensing portions are formed to said each pixeland has an opening for light incidence to said one or more light sensing portionsAbout each of all or a part of pixels of said two or more pixelsthe perimeter of said opening corresponding to at least one of said one or more light sensing portions corresponding to the pixel concerned

meets in part at leastA solid state camerawherein an oblique light reflection part which reflects a part of oblique light which is the light which enters aslant from the opening concerned in a height position between at least one light sensing portion concerned and said light-shielding film is formed.

[Claim 2]The solid state camera according to claim 1wherein said oblique light reflection part is formed along with the whole substantially [perimeter / said].

[Claim 3]The solid state camera according to claim 1 or 2 characterized by the side of said reflecting layer reflecting said a part of oblique light including a reflecting layer which comprised material as an electrode layer or a wiring layer located in a downward height position to said light-shielding film with said same oblique light reflection part.

[Claim 4]The solid state camera according to any one of claims 1 to 3wherein said at least a part of oblique light reflection part is used also [which is located in a downward height position to said light-shielding film / an electrode layer or a wiring layer].

[Claim 5]The solid state camera according to any one of claims 1 to 3wherein said oblique light reflection part separated from an electrode layer or a wiring layer located in a downward height position to said light-shielding film and is formed.

[Claim 6]The solid state camera according to any one of claims 1 to 5wherein said at least a part of oblique light reflection part forms through hole structure.

[Claim 7]The solid state camera according to any one of claims 1 to 6wherein said oblique light reflection part has been arranged so that it may become abbreviated ******** centering on a center position of said opening corresponding to the oblique light reflection part concerned.

[Claim 8]According to a position of a pixel corresponding to the oblique light reflection part concernedsaid oblique light reflection partArrangement of the oblique light reflection part concerned to said opening corresponding to said oblique light reflection part corresponding to at least one of pixels which arrangement of the oblique light reflection part concerned to said opening corresponding to the oblique light reflection part concerned is definedand is said two or more pixelsThe solid state camera according to any one of claims 1 to 6wherein arrangement of the oblique light reflection part concerned to said opening corresponding to said oblique light reflection part

corresponding to at least one pixel of others of said two or more pixels differs.
[Claim 9]Two or more photoelectric conversion parts which it is two or more photoelectric conversion parts arranged in the shape of two dimensionsand each generates a signal charge according to incident lightand are accumulatedTwo or more amplifiers which it is two or more amplifiers provided corresponding to said two or more photoelectric conversion partsand each has regulatory regionand produce a signal output according to an electric charge of this regulatory regionTwo or more transfer parts which transmit a signal charge which were two or more transfer parts provided corresponding to said two or more photoelectric conversion partswas generatedrespectively and was accumulated by said two or more photoelectric conversion parts to said regulatory region of two or more of said amplifiersrespectivelyTwo or more wiring in which each was provided for every line of two or more of said photoelectric conversion partsand two or more semiconductor regions provided corresponding to said two or more amplifiersThey are two or more switching elements which are provided for every line of two or more of said photoelectric conversion partsand control electric connection and interception between a semiconductor region of said plurality corresponding to the line concernedand said regulatory region of two or more of said amplifiers corresponding to the line concernedEach is provided with two or more switching elements which make said regulatory region of either of said two or more semiconductor regions corresponding to the line concernedand either of said two or more amplifiers corresponding to the line concerned a main electrode regionrespectivelyand them at least one semiconductor region of two or more of said whole semiconductor regionsWhen it is formed so that a signal charge according to incident light may be generatedand said two or more switching elements corresponding to the line concerned are in switch-on for every line of two or more of said photoelectric conversion partsWhile being in the state where said regulatory region of two or more of said amplifiers corresponding to the line concerned was electrically connected to said wiring corresponding to the line concernedWhen said two or more switching elements corresponding to the line concerned are in a cut off stateIt will be in the state where said regulatory region of two or more of said amplifiers corresponding to the line concerned was electrically intercepted to said wiring corresponding to the line concernedAbout each line to which

said at least one semiconductor region relates among lines of two or more of said photoelectric conversion parts. When said two or more switching elements corresponding to the line concerned are in switch-onIt will be in the state where said at least one semiconductor region was electrically connected to said wiring corresponding to the line concernedSaid photoelectric conversion part constitutes one of said one or more light sensing portions formed to said pixel. Said at least one semiconductor region formed so that a signal charge according to said incident light might be generated constitutes one light sensing portion of others of said said one or more light sensing portions formed to said pixel. The solid state camera according to any one of claims 1 to 8 characterized by things.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to a solid state camera.

[0002]

[Description of the Prior Art]Beforesolid state camerassuch as CCDa CMOS image sensorand an amplified type image sensorare providedfor example as an image input element of an electronic camera.

[0003]In such conventional various solid state camerasit has two or more pixelsone or more light sensing portions are formed to said each pixeland it has a light-shielding film with the opening for light incidence to said one or more light sensing portions.

[0004]

[Problem to be solved by the invention]Howeverin the conventional solid state camerait did not have the structure considered about the oblique light which is the light which enters aslant from the opening of said light-shielding filmbut when a part of oblique light also reached the portion around a light sensing portionvarious inconvenience had arisen. Generating of a smearthe fall of sensitivityetc. can be mentioned as these inconvenient examples. If said other inconvenient examples are explainedfor example like the solid state camera currently indicated by JPH11-204769A etc.In the solid state camera provided also with the light sensing portion for an incident-light-quantity monitor besides the light sensing

portion for an image pick-up which receives original incident light in order to obtain a video signal. There was a case where the optical generating electric charge produced according to a part of oblique light which entered from the opening corresponding to the light sensing portion for an image pick-up mixed to the optical generating electric charge which should be essentially acquired from the light sensing portion for an incident-light-quantity monitorand it became impossible to monitor incident light quantity with sufficient accuracy. The inconvenience explained above becomes remarkable as the density of a light sensing portion increases by raising the degree of location of a pixel or providing two or more light sensing portions to one pixel.

[0005]This invention was made in view of such a situationand an object of this invention is to provide the solid state camera which can reduce the inconvenience accompanying the entering oblique light.

[0006]

[Means for solving problem]In order to solve said problemthe solid state camera by the 1st mode of this inventionIn the solid state camera which has a light-shielding film which it has two or more pixelsand one or more light sensing portions are formed to said each pixeland has an opening for light incidence to said one or more light sensing portionsAbout each of all or a part of pixels of said two or more pixelsthe perimeter of said opening corresponding to at least one of said one or more light sensing portions corresponding to the pixel concerned meets in part at least (the thing of the perimeter met not less than 30% is preferredand). The thing of the perimeter met not less than 50% is more preferredand the thing of the perimeter met not less than 70% is much more preferred. In the height position between at least one light sensing portion concerned and said light-shielding filmthe oblique light reflection part which reflects a part of oblique light which is the light which enters aslant from the opening concerned is formed.

[0007]Since the oblique light reflection part is formed according to this 1st modeit is reflected by an oblique light reflection partand a part of oblique light enters into a light sensing portion. Thereforewhile the quantity of the oblique light which enters into the portion around a light sensing portion is reducedthe light volume which enters into a light sensing portion increasesand sensitivity increases. As a resultthe inconvenience accompanying the entering oblique light is reduced. For

examplea smear is reducedsensitivity increases and the monitor accuracy of incident light quantity increases depending on the case.
[0008]In said 1st modealthough an oblique light reflection part may be formed about two or more pixelsan oblique light reflection part may be formed only about a pixel of a peripheral side of a field over which said two or more pixels are distributedfor example. Since an optic axis of an image formation lens is set up near the center of said field when this carries the solid state camera concerned in an electronic camerafor exampleWhile light which does not have almost inclination in a pixel near the center of said field enterssince distance from an optic axis of said lens becomes largein a pixel of a peripheral sideit is because inclination of entering light becomes large.
[0009]A solid state camera by the 2nd mode of this invention is formed along with the whole in said 1st mode substantially [reflection part / said / oblique light / perimeter / said].
[0010]In this 2nd modesince an oblique light reflection part is formed along with the whole substantially [perimeter / said]while being able to reduce further quantity of an oblique light which enters into a portion around a light sensing portion irrespective of direction of an oblique lightlight volume which enters into a light sensing portion increases moresensitivity increases furtherand it is desirable.
[0011]The side of said reflecting layer reflects said a part of oblique light including a reflecting layer which comprised material as an electrode layer or a wiring layer to which said oblique light reflection part is located in a downward height position to said light-shielding film in said 1st or 2nd mode with same solid state camera by the 3rd mode of this invention.
[0012]Since the material of the reflecting layer which constitutes at least a part of oblique light reflection part comprises same material (for examplematerial which uses aluminum as the main ingredients) as said electrode layer or a wiring layer according to this 3rd modeSaid wiring layer can be formed when manufacturing the solid state camera concerned by the same manufacturing process as said electrode layer or a wiring layer. For this reasonan oblique light reflection part can be formed easily and a cost cut can be aimed at.
[0013]The solid state camera by the 4th mode of this invention is used also [to which said at least a part of oblique light reflection part is located in a downward

height position to said light-shielding film / the electrode layer or wiring layer] in said 1st [the] thru/or the 3rd one of modes.
[0014]Since at least a part of oblique light reflection part is used also [wiring layer / said electrode layer or] according to this 4th modestructure becomes easy and a cost cut can be aimed at.
[0015]In said 1st [the] thru/or the 3rd one of modessaid oblique light reflection part separates the solid state camera by the 5th mode of this invention from the electrode layer or wiring layer located in a downward height position to said light-shielding filmand it is formed.
[0016]In said 1st [the] thru/or the 3rd modelike said 4th modealthough at least a part of oblique light reflection part may be used also [wiring layer / said electrode layer or]the oblique light reflection part may be separated from said electrode layer or the wiring layer like said 5th mode.
[0017]In said 1st [the] thru/or the 5th one of modesas for the solid state camera by the 6th mode of this inventionsaid at least a part of oblique light reflection part forms through hole structure. Herealthough through hole structure means the same structure as a through holeany may be sufficient as the existence of the function of an electrical link.
[0018]Since through hole structure is adopted according to this 6th modeThe area of the effective reflector in an oblique light reflection part can be increasedthe reflected amount to an oblique light can be increasedthe light volume which enters into a light sensing portion while being able to reduce further the quantity of the oblique light which enters into the portion around a light sensing portion increases moresensitivity increases furtherand it is desirable. The through hole structure of an oblique light reflection part can also be formed when manufacturing the solid state camera concerned by the same manufacturing process as the through hole about the electrode layer or wiring layer located in a downward height position to a light-shielding film. For this reasonan oblique light reflection part can be formed easily and a cost cut can be aimed at.
[0019]In said 1st [the] thru/or the 6th one of modesthe solid state camera by the 7th mode of this invention is arranged so that said oblique light reflection part may serve as abbreviated ******** centering on the center position of said opening corresponding to the oblique light reflection part concerned.
[0020]Although direction of an oblique light which enters

into an opening according to a position of a pixel differsif an oblique light reflection part is arranged like said 7th mode so that it may become abbreviated ********dispersion in the reflection property (reflected amount of an oblique light reflection part) of an oblique light reflection part by a position of a pixel can be reducedand it is desirable. And since it becomes possible to make the same arrangement to an opening of an oblique light reflection part also about which pixel according to said 7th modea design pattern etc. become easy.

[0021]In said 1st [the] thru/or the 6th one of modesa solid state camera by the 8th mode of this invention the (a) aforementioned oblique light reflection partAccording to a position of a pixel corresponding to the oblique light reflection part concernedarrangement of the oblique light reflection part concerned to said opening corresponding to the oblique light reflection part concerned is defined(b) Arrangement of the oblique light reflection part concerned to said opening corresponding to said oblique light reflection part corresponding to at least one pixel in said two or more pixelsArrangement of the oblique light reflection part concerned to said opening corresponding to said oblique light reflection part corresponding to at least one pixel of others of said two or more pixels differs.

[0022]By this 8th mode as well as said 7th modedispersion in the reflection property (reflected amount of an oblique light reflection part) of an oblique light reflection part by a position of a pixel can be reducedand it is desirable.

[0023]In said 1st [the] thru/or the 8th one of modes a solid state camera by the 9th mode of this inventionTwo or more photoelectric conversion parts which it is two or more photoelectric conversion parts arranged in the shape of two dimensionsand each generates a signal charge according to incident lightand are accumulatedTwo or more amplifiers which it is two or more amplifiers provided corresponding to said two or more photoelectric conversion partsand each has regulatory regionand produce a signal output according to an electric charge of this regulatory regionTwo or more transfer parts which transmit a signal charge which were two or more transfer parts provided corresponding to said two or more photoelectric conversion partswas generatedrespectively and was accumulated by said two or more photoelectric conversion parts to said regulatory region of two or more of said amplifiersrespectivelyTwo or more wiring in which each was provided for every line of two or more of said photoelectric conversion partsand two

or more semiconductor regions provided corresponding to said two or more amplifiersThey are two or more switching elements which are provided for every line of two or more of said photoelectric conversion partsand control electric connection and interception between a semiconductor region of said plurality corresponding to the line concernedand said regulatory region of two or more of said amplifiers corresponding to the line concernedEach is provided with two or more switching elements which make said regulatory region of either of said two or more semiconductor regions corresponding to the line concernedand either of said two or more amplifiers corresponding to the line concerned a main electrode regionrespectively. (a) at least one semiconductor region of two or more of said whole semiconductor regionsWhen it is formed so that a signal charge according to incident light may be generatedand said two or more switching elements corresponding to the line concerned are in switch-on for every line of a photoelectric conversion part of the (b) aforementioned pluralityWhile being in the state where said regulatory region of two or more of said amplifiers corresponding to the line concerned was electrically connected to said wiring corresponding to the line concernedWhen said two or more switching elements corresponding to the line concerned are in a cut off stateIt will be in the state where said regulatory region of two or more of said amplifiers corresponding to the line concerned was electrically intercepted to said wiring corresponding to the line concerned(c) About each line to which said at least one semiconductor region relates among lines of two or more of said photoelectric conversion parts. When said two or more switching elements corresponding to the line concerned are in switch-onIt will be in the state where said at least one semiconductor region was electrically connected to said wiring corresponding to the line concerned(d) Said at least one semiconductor region formed so that said photoelectric conversion part might constitute one of said one or more light sensing portions formed to said pixel and a signal charge according to the (e) aforementioned incident light might be generatedOne light sensing portion of others of said said one or more light sensing portions formed to said pixel is constituted.

[0024]. As [indicated / this 9th mode / in said 1st / the / thru/or the 8th mode / by JPH11-204769A] It is the example applied to the solid state camera provided also with the light sensing portion for an incident-light-quantity monitor (said semiconductor region) besides the

light sensing portion for an image pick-up (said photoelectric conversion part) which receives incident light original for an image pick-up. According to this 9th modeit also becomes possible toacquire the effect of being able to monitor incident light quantity with sufficient accuracy for example.
[0025]
[Mode for carrying out the invention]Hereafterthe solid state camera by this invention is explained with reference to Drawings.
[0026][A 1st embodiment]
[0027]Drawing 1 is an outline top view showing typically the unit pixel of the solid state camera by a 1st embodiment of this invention. Drawing 2 is the outline sectional view which met X1-X2 line in drawing 1. Drawing 3 is the outline sectional view which met Y1-Y2 line in drawing 1. Drawing 4 is the outline sectional view which met Y3-Y4 line in drawing 1. Drawing 5 is a circuit diagram showing the equivalent circuit of this unit pixel.
[0028]The solid state camera by this embodiment has the composition with which the unit pixel shown in drawing 1 thru/or drawing 5 was arranged by the two-dimensional matrix (mxn). The photo-diode 1 as a photoelectric conversion part which generates and accumulates the signal charge according to incident light as this unit pixel is shown in drawing 1 thru/or drawing 5The junction field effect transistor (henceforth "JFET") 2 as an amplifier which produces the signal output (amplified output) according to the electric charge of the gate region 15 as regulatory regionThe transfer gate 3 which consists of polysilicon as a transfer part which transmits the signal charge generated and accumulated with the photo-diode 1 to the gate region 15 of JFET2The reset drain wiring 24 as wiring in which driving signal phiRSD for controlling the potential of the gate region 15 concerned while making the electric charge of the gate region 15 of JFET2 discharge is suppliedThe reset drain 4 as a P type diffusion layer (P-type semiconductor region) provided corresponding to JFET2It is P channel MOSFET9 which is the insulated gate type transistors as a switching element which controls the electric connection and interception between this reset drain 4 and the gate region 15 of JFET2P channel MOS FET9 which uses the reset gate 5 as a control electrode while making the reset drain 4 of the pixel concernedand the gate region 15 of JFET2 of the pixel concerned into a main electrode regionrespectivelyPreparation ******.
[0029]Said photo-diode 1JFET2and the reset drain 4It is

formed into the low concentration N type epitaxial layer 11 formed in the main table side side upper part of the N type high concentration silicon substrate 10and the transfer gate 3 and the reset gate 5 are formed via the insulator layer 33 on the N type epitaxial layer 11.
[0030]The P type charge storage field 12 formed into the N type epitaxial layer 11 as the photo-diode 1 was shown in drawing 3 and drawing 4It comprises the high-concentration N-type semiconductor field 13 formed near the semiconductor surface of the P type charge storage field 12 upper partand the N type epitaxial layer 11and has become a photo-diode of a flush type.
[0031]The gate region 15 which consists of a P type diffusion layer formed into the N type epitaxial layer 11 as JFET2 is shown in drawing 2 and drawing 3High-concentration N type source region 14 and the N type channel regions 17 which were formed all over this P type gate region 15It comprises a drain area which consists of a portion of the N type epitaxial layer 11 of a position which faces the source region 14 across the channel regions 17an electric charge of the photo-diode 1 is received in the gate region 15and this is amplified and outputted.
[0032]As shown in drawing 1drawing 3and drawing 4the high-concentration N type diffusion layer 16 used as the isolation region between the pixels which adjoin mutually is continuously formed in the peripheral region of a pixel with N type source region 14 and the N type epitaxial layer 11 which constitute the photo-diode 1. ThereforeN type region (1113) of the PN junction which constitutes the photo-diode 1and the N type drain region (a part of N type epitaxial layer 11) of JFET are electrically connected.
[0033]The P type gate region 15 of JFET2 is formed so that it may face across the N type channel regions 17 from the upper and lower sidesit suppresses a board bias effectand it has structure which oppresses gain dispersion at the same time it raises the gain of source follower operation.
[0034]The transfer gate 3 comprises a gate electrode formed via the insulator layer 33 on a border area of the P type charge storage field 12 of the photo-diode 1and the P type gate region 15 of JFET2as shown in drawing 3An electric charge accumulated in the P type charge storage field 12 of the photo-diode 1 is transmitted to the P type gate region 15 of JFET2.
[0035]That isP channel MOS FET comprises a P type region (P type charge storage field 12) of a PN junction which constitutes the photo-diode 1the transfer gate 3and the P type gate region 15 of JFET2.

[0036]. As the reset drain 4 was shown in drawing 2 and drawing 4were formed into the N type epitaxial layer 11. An electric charge which comprised a P-type semiconductor regionand generation accumulation was carried out with the photo-diode 1and was transmitted to the P type gate region 15 of JFET2 is dischargedPotential of the P type gate region 15 of JFET2 is controlled via the reset gate 5 (namelyP channel MOS FET9 which has the reset gate 5).
[0037]The reset gate 5 comprises a gate electrode formed via the insulator layer 33 on a border area with the reset drain 4 which is the P type gate region 15 and a P-type semiconductor region of JFET2as shown in drawing 2An electric connectable state of the P type gate region 15 of JFET2 and the reset drain 4 is controlled. That isas mentioned aboveP channel MOS FET9 comprises the P type gate region 15 of JFET2the reset gate 5and the reset drain 4. This MOSFET9 is using the reset gate 5 as a control electrode while making the reset drain 4 of the pixel concernedand the gate region 15 of JFET2 of the pixel concerned a main electrode regionrespectively.
[0038]On a border area of the P type gate region 15 of JFET2 of the pixel concernedand the reset drain 4 of an adjacent pixel of one side of a line writing directionthe gate electrode (gate electrode of left-hand side in drawing 1 and drawing 2) 5a is formed via the insulator layer 33. On a border area of the reset drain 4 of the pixel concernedand the P type gate region 15 of JFET2 of an adjacent pixel of the other side of a line writing directionthe gate electrode (gate electrode of right-hand side in drawing 1 and drawing 2) 5a is formed via the insulator layer 33. that isIf the P type gate region 15 of JFET2 of the pixel concerned and the reset drain 4 of an adjacent pixel of one side of a line writing direction are made into a main electrode regionrespectively. Drawing 1 as a switching element between pixels which both use the gate electrode 5a of left-hand side in drawing 1 as a control electrodeand P channel MOSFET9a of left-hand side in drawing 2It reachesIf the reset drain 4 of the pixel concerned and the P type gate region 15 of JFET2 of an adjacent pixel of the other side of a line writing direction are made into a main electrode regionrespectively. P channel MOS FET9a of drawing 1 as a switching element between pixels which both use the gate electrode 5a of right-hand side in drawing 1 as a control electrodeand right-hand side in drawing 2 is formed. The gate electrodes 5a and 5a are continuously formed with polysilicon with the reset gate wiring 21 as well as the reset gate 5and the

gate electrodes 5a and 5a and the reset gate 5 are connected in common by the reset gate wiring 21 concerned.
[0039]The overflow control field 6 which leads the electric charge superfluously generated with the photo-diode 1 to the reset drain 4 is formed. The overflow control field 6 The P type charge storage field 12 of the photo-diode 1It consists of a P-type semiconductor region formed in N type epitaxial layer 11 inside of a border area with the reset drain 4and the overflow operation which leads the electric charge superfluously generated with the photo-diode 1 to the reset drain 4 is controlled. Near the semiconductor surface of the overflow control field 6 upper partthe high-concentration N-type semiconductor field 16 mentioned above is formed. Namelythe P type charge storage field 12 of the photo-diode 1the P type overflow control field 6and the reset drain 4P channel JFET which considered it as the source regionchannel regionsand a drain areaand made the gate region the high-concentration N-type semiconductor field 16 and the N type epitaxial layer 11respectively is formed. This P channel JFET is in a cutoff (interception) statewhen the photo-diode 1 is carrying out standard operationand a light strong against the photo-diode 1 entersIf the electric charge (in this casepositive charge by a hole) more than the constant rate in the P type charge storage field 12 is accumulatedit will be got blockedand if it goes up more than a level with the potential of the P type charge storage field 12it is formed so that it may be in a conduction (one) state. Thereforethe electric charge generated superfluously flows into the reset drain 4 via the overflow control field 6 with the photo-diode 1. These excess charges are discharged from the reset drain wiring 24 via a predetermined course. The high-concentration N-type semiconductor field 16 formed near the semiconductor surface of the overflow control field 6 upper part is continuously formed with the high-concentration N-type semiconductor field 13 formed near the surface of the photo-diode 1. Thereforethe neighborhood of a semiconductor surface of the P type charge storage field 12 of the photo-diode 1 serves as structure covered in the high-concentration N-type semiconductor field (13 and 16) also including a peripheral regionand the photo-diode 1 is an embedding photo-diode. Although the high-concentration N-type semiconductor field (13 and 16) is not formed in the end by the side of the transfer gate 3 of the photo-diode 1and the transfer gate 3 lower part on structurethe performance (low dark current characteristic by depletion[non-]-izing of a semiconductor surface) of an

embedding photo-diode is held. During the period whenas for thisthe photo-diode 1 is performing accumulation operation of the signal charge by photoelectric conversionIt is because are in an interception (OFF) statehigh-level pulse voltage is impressedan electron is induced near the semiconductor surface of this field as a result and the transfer gate 3 is made into a high-concentration N-type semiconductor field. Thusthe photo-diode 1 is a JFET type horizontal-type overflow drain structure the embedding type photo-diode which it hadand by overflow structure. Since the depletion layer produced in a PN junction part does not reach a semiconductor surface with an embedding photo-diode while being able to oppress the phenomenon of a blot of bloominga smearetc.dark current is oppressed. In order that an electric charge may not remain in a photo-diode after an electric charge is transmitted (based on full transmission or perfect depletion-ization)the ideal characteristic which stopped the afterimage and the reset noise is obtained.

[0040]In additionthe transfer gate wiring 20 which consists of polysiliconthe reset gate wiring 21 which consists of polysiliconthe reset drain wiring 24 which consist of the 2nd layer Al film and which was mentioned aboveand the vertical signal wire (source wiring of JFET2) 22 by the 1st layer Al film are also formed as shown in a figure. NamelyN type source region 14 of each JFET2 is connected in common to vertical scanning directions (line direction) by the vertical signal wire 22 for every sequence. In the transfer gate 3the reset gate 5 is connected in common to the horizontal scanning direction (line writing direction) by the reset gate wiring 21 the whole line with the transfer gate wiring 20respectively.

[0041]According to this embodimentthe reset drain wiring 24 is made to serve a double purpose as a light-shielding film. While the opening 24a for light incidence is formed in the field corresponding to the photo-diode 1the opening 24b for light incidence is formed in the field corresponding to the reset drain 4 at the reset drain wiring 24. The reset drain wiring 24 as a light-shielding film covers the field except the photo-diode 1 and the reset drain 4and is shading this field. Although the reset drain wiring 24 is not shown in Drawingsit is electrically connected to the reset drain 4 of any one or more horizontal pixels for every line.

[0042]The reset drain 4 is a P-type semiconductor regionas mentioned aboveand the N-type semiconductor field (N type epitaxial layer) 11 is arranged under thisSince reverse bias of the reset drain 4 and the N-type semiconductor field 11 is always carried out (VDD>phi RSD)the reset drain

4 commits them as photo-diode 40 with the another photo-diode 1 as a photoelectric conversion part. In this photo-diode 40the photoelectric current by the signal charge (this example hole) by which it was generated according to the light which entered into the opening 24b occurs. That isin this embodimentthe reset drain 4 as a semiconductor region is formed so that the signal charge according to incident light may be generated. Thusin this embodimentto one pixelin order to obtain a video signalthe photo-diode 40 as a light sensing portion for an incident-light-quantity monitor is also formed besides the photo-diode 1 as a light sensing portion for an image pick-up which receives original incident light.

[0043]And in this embodimentas shown in drawing 1 and drawing 4in between the photo-diode 1 and the photo-diodes 40the oblique light reflecting film 60 which consists of the 1st layer Al film is formed in the height position between the photo-diodes 1 and 40 and the light-shielding film (reset drain wiring) 24. The both side surfaces of the oblique light reflecting film 60 meet a part of perimeter of the opening 24a (it corresponds to the photo-diode 1) of the wiring 24 of the light-shielding film 24and a part of perimeter of the opening 24b (it corresponds to the photo-diode 40)respectivelyand form the oblique light reflectorrespectively. Between the oblique light reflecting film 60 and the light-shielding film 24while the grooved through hole 61 where it filled up with tungsten along with a part of perimeter of the opening 24a is formedthe grooved through hole 62 where it filled up with grooved tungsten along with a part of perimeter of the opening 24b is formed. The oblique light reflecting film 60 and the through hole 61 constitute the oblique light reflection part formed along with a part of perimeter of the opening 24a from this embodiment. The oblique light reflecting film 60 and the through hole 62 constitute the oblique light reflection part formed along with a part of perimeter of the opening 24b.

[0044]An operation of these oblique light reflection parts is explained in full detail behind.

[0045]Drawing 6 is a circuit diagram showing the solid state camera by this embodiment which arranged the unit pixel shown in drawing 1 thru/or drawing 5 to the two-dimensional matrix (mxn).

[0046]Each pixel used as a unit pixel so that the explanation about the structure mentioned above may also showTwo P channel MOSFET9a over JFET2the transfer gate 3and the 5 adjacent pixel reset gate that exists in [one] 4 or

1 pixel of reset drains by halvesIn order to obtain a video signalit comprises the photo-diode 1 as a light sensing portion for an image pick-up which receives original incident lightand the photo-diode 40 as a light sensing portion for an incident-light-quantity monitor. As a switching element which controls the electric connection and interception between the reset drain 4 and the gate region 15 of JFET2The P channel MOS transistor 9 which comprises the gate region 15the reset gate 5and the reset drain 4 of JFET2 exists in [one] 1 pixel. These are electrically connectedas shown in drawing 5.

[0047]The source region (S) 14 which is every JFET2 is connected in common by the vertical signal wire 22-1 - 22-n (equivalent to the vertical signal wire 22 in drawing 5) for every sequence of matrix arrangementrespectively.

[0048]The drain area (D) which is every JFET2 is connected to the drain power supply VDD by the N type epitaxial layer 11 [all the / pixel].

[0049]For every line of matrix arrangementit is connected by the transfer gate wiring 20-1 - 20-m (equivalent to the transfer gate wiring 20 in drawing 5) common to a horizontal scanning directionand the transfer gate 3 is connected to the vertical scanning circuit 7. And it operates for every line by drive pulse phiTG1 sent out from the vertical scanning circuit 7 - phiTGm.

[0050]In each line of matrix arrangementthe reset drain 4 and the gate region 15 of JFET2 are arranged by turns at a line writing direction (horizontal scanning direction)the gate electrode 5a is altogether arranged between each pixeland said P channel MOS FET9a is formed. In each line of matrix arrangementthe gate electrode 5a between all the reset gates 5 in the pixel of the line concernedand the pixel of the line concernedIt is altogether connected by the reset gate wiring 21 common to a line writing direction for every lineand by drive pulse phiRSG1 sent out from the vertical scanning circuit 7 - phiRSGmit will operate for every line and P channel MOS FET 9 and 9a as a switching element of the line concerned will be altogether turned on and off simultaneously.

[0051]For this reasonsince the reset drain wiring 24 is electrically connected to the reset drain 4 of any one or more horizontal pixels for every lineso that drawing 6 may also showWhen the one [all the MOSFETs 9 and 9a of the line concerned] (it is in switch-on) for every lineIt will be in the state where the gate region 15 and the reset drain 4 of JFET2 of the line concerned were electrically connected to the reset drain wiring 24 of the line

concerned[of all the pixels] The gate region 15 and the reset drain 4 of all the JFET2 of the line concerned are electrically connected by P channel MOS FET9a between pixels. Thereforethe reset drain 4 will be in the state where it was electrically connected to the reset drain wiring 24 of the line concerned also about the gate region 15 of JFET2 of the pixel which is not directly connected to the reset drain wiring 24. When all the MOSFETs 9 and 9a of the line concerned turn off for every line (it is in a cut off state)it will be in the state where the gate region 15 of JFET2 of all the pixels of the line concerned was electrically intercepted to the reset drain wiring 24 of the line concerned.

[0052]Thereforeby giving driving signal phiRSD for controlling the potential of the gate region 15 concerned for every linewhile making the reset drain wiring 24 of the line concerned discharge the electric charge of the gate region 15 of JFET2This signal can be given to the gate region 15 of JFET2 of all the pixels of the line concerned.

[0053]About each linewhen one [all the P channel MOS FET 9 and 9a of the line concerned]Since the gate region 15 and the reset drain 4 of all the JFET2 of the line concerned are electrically connected by P channel MOS FET9a between pixelsthe reset drain 4 of the line concernedIt will be in the state where it was electrically connected to the reset drain wiring 24 of the line concernedvia P channel MOSFET9a of the line concernedand the reset drain 4. Thereforethe photoelectric current by the signal charge (this embodiment hole) by which it was generated according to the light which entered from said opening 24b can be made to output from the reset drain wiring 24 of the line concerned.

[0054]About each linethe reset drain wiring 24 of each line concernedIt is connected to the outputting part of each drive pulse phiRSD of the line of the vertical scanning circuit 7 concerned via switch QA which consists of MOSFETs etc.respectivelyrespectivelyand the switch QB is further connectedrespectively between the reset drain 24 of each line concernedand the light volume monitor signal output terminal 50. Drive pulse phiPD is impressed to the gate electrode of each switch QAand the pulse which reversed drive pulse phiPD at the knot gate 51 is impressed to the gate electrode of each switch QB. In this embodimentsaid each switch QA and each switch QB to the reset drain wiring 24 of each line. The state where driving signal phiRSD for controlling the potential of the gate region 15 concerned while making the electric charge of the gate region 15 of JFET2 of each pixel of the line concerned discharge is

suppliedThe switching part which changes the state of making the signal which appeared in the wiring 24 concerned outputting from the reset drain wiring 24 of the line concerned is constituted. Thereforein this embodimentthe photoelectric current Ip generated in the reset drain 4 of each pixel can be outputted to the element exterior from the terminal 50 via the switch QB.

[0055]It is connected to the constant current source 26-1 - 26-n in one sideconstant current flows from the constant current source 26-1 - 26-n by thisand the vertical signal wire 22-1 - 22-n constitute the source follower circuit from JFET4and the constant current source 26-1 - 26-n. It is connected to the output side of this source follower circuit at the difference processing circuit 27-1 as readout circuitry - 27-nrespectively. The difference processing circuit 27-1 - 27-n comprise the capacity 28-1 - 28-nand the switches 29-1such as MOSFET- 29-n. Common connection of the gate of the switch 29-1 - 29-n is carried outand it operates by pulse phiN. The outputting part of the difference processing circuit 27-1 - 27-n is connected to the signal output line 34 via the level selecting switch 39-1 - 39-n. The level selecting switch 39-1 - 39-n operate sequentially by the pulse phiH1 sent out from the horizontal scanning circuit 8 - phiHnand make the output of the difference processing circuit 27-1 - 27-n output to the signal output line 34 one by one. This output is outputted outside via the output amplifier 35 connected to the signal output line 34. The output signal line 34 is grounded via the switch 36. This switch 36 operates by pulse phiRH.

[0056]Nextthe drive timing chart of the shutter of the solid state camera and the camera concerned in the case of picturizing Still Picture Sub-Division using the single lens reflex camera digital still camera etc. which carry the solid state camera by this embodiment is shown in drawing 7.

[0057]In the period T1a of the first half within the period T1the transfer gate 3 of all the pixels is turned on and offthe electric charge of the photo-diode 1 which are all the pixels is transmitted to the gate region 15 of JFET2and the photo-diode 1 is reset. Since each drive pulse phiRSD serves as the voltage VGHeach drive pulse phiRSG serves as a low level at this time and P channel MOS FET 9 and 9a is turned on altogetherthe gate region 15 of JFET2 is set as the voltage VGH.

[0058]Nexteach drive pulse phiRSD is made high-level in the period T1b of the second half within the period T1Also at this timesince P channel MOS FET 9 and 9a is turned on

altogetherthe gate region 15 of JFET2 of all the pixels is set as the voltage VGL (potential which makes JFET4 turn off)initialization of a pixel is completedand preparation included in an exposed state is completed.
[0059]In the period T2the shutter 101 will open and it will be in an exposed state. P channel MOS FET 9 and 9a of the line containing said 1st pixel that has a function which monitors light volume at this time is turned on altogetherAnd since pulse phiPD is a low leveland and switching QA turns offit has changed to the state where the reset drain wiring 24 was connected to the output terminal 50. [the switch QB] As a resultthe photoelectric current Ip generated in each pixel flows into the photoelectric current integration circuit (not shown) of a shutter control circuitand the output voltage Vip changesas shown in drawing 7. Since inclination of the voltage Vip is proportional to the incident light intensity to the solid state camera 15when it monitors the voltage Vipwhile exposing a desired light exposureit can ask in real time. That iswhen the output voltage Vip of a photoelectric current integration circuit exceeds the reference voltage Vc by drawing 7a control signal is sent from a shutter control circuitand a shutter is closed. Theneach line is read one by one.
[0060]Since one [period T3 / the switch QB turns off and / switching QA]the reset drain wiring 24 has changed to the vertical scanning circuit 7 side. Since P channel MOS FET 9 and 9a is altogether turned on at this timethe gate region 15 of JFET2 is set as the voltage VGHand after thatP channel MOS FET 9 and 9a turns it offand it is made floating by drive pulse phiRSD of the line concerned.
[0061]In the period T4a signal is read from the source region 14 of JFET2 in source follower modeand it is held as the reference signal (dark output) Vref at the capacity 28 of the difference processing circuit 27. And if pulse phiN becomes a low and the switch 29 turns offthe output side (29 sides) of the capacity 28 will become floating.
[0062]In the period T5the lightwave signal electric charge accumulated in the photo-diode 1 is transmitted to the gate region 15 of JFET2 via the transfer gate 3. Since the output side of the capacity 28 is floating at this timedifference signal Vs-Vref of the lightwave signal (bright output) Vs and the reference signal (dark output) Vref read from the source region 14 of JFET2 (S) appears.
[0063]In the period T6one by one with the horizontal scanning circuit 8and difference signal Vs-Vref which is each pixel of the line concerned is read from capacity 28-i

as a picture signaland is outputted from the output terminal OUT via the output amplifier 35. [the level selecting switch 39]
[0064]Said period T3 - T6 are successively repeated about each line.
[0065]Thussince the solid state camera by this embodiment can monitor the light volume which carries out direct entering to a solid state camera during exposure in real timeeven if incident light quantity changesit can be picturized by the always optimal exposure time at the digital still camera using the solid state camera concerned. About the case where a stroboscope is usedsimilarlyTTL modulated light can be carried out and it can picturize by the optimal exposure time.
[0066]Herethe solid state camera as a comparative example shown in drawing 8 thru/or drawing 11 is compared and explained about the technical meaning of the oblique light reflection part (the oblique light reflecting film 60the through holes 61 and 62) mentioned above.
[0067]Drawing 8 thru/or drawing 11 support drawing 1 thru/or drawing 4respectively. In drawing 8 thru/or drawing 11identical codes are given to an element which is the same as an element in drawing 1 thru/or drawing 4or correspondsand the overlapping explanation is omitted to it. A place where a solid state camera shown in drawing 8 thru/or drawing 11 differs from a solid state camera by this embodiment is only the point that an oblique light reflection part (the oblique light reflecting film 60the through holes 61 and 62) is not formed.
[0068]As shown [this comparative example] in drawing 9while monitoring the light volume of the incident light 100 which entered aslanta part of oblique-incidence light component among the incident light 100 which passed the opening 23. Will pass through the reset gate 5 which consists of polysiliconan optical generating electric charge will be made incorrect-mixed to JFET2and it will become impossible to grasp incident light quantity correctly as a light volume monitor.
[0069]In this comparative exampleas shown in drawing 10while monitoring light volumeat the time of the both sides of the between at the time of this photographythe electric charge generated by the incident light which passed through the transfer gate 3 which consists of polysilicon will incorrect-mix to JFET2. Thereforewhile monitor accuracy fallsthe sensitivity lowering under this photography will be brought about.
[0070]In this comparative examplelike [as shown in drawing

11] the case of drawing 9 mentioned aboveA part of oblique-incidence light component among the lights which were going to face monitoring light volumewere going to pass the opening 24aand were originally going to enter into the reset drain 4. Pass the reset gate wiring 21 which consists of polysiliconand the generating electric charge incorrect-mixes via the P type lateral overflow drain diffusion zone 6 to the P type charge storage field 12 (field 12 which appeared the left end in drawing 11) of the photo-diode 1 of an adjacent pixelIt will become impossible to grasp incident light quantity correctly as a light volume monitor. In additionthe inside of the incident light 100 which passed the opening 24b and carried out oblique incidence to the photo-diode 1While the electric charge generated by the light which passed the transfer gate wiring 20 and invaded will incorrect-mix to the reset drain 4 which constitutes the photo-diode 40 and making the output as a light volume monitor inaccuratethe sensitivity lowering under this photography will be brought about.
[0071]On the other handaccording to this embodimentalthough the situation of drawing 2 and drawing 3 is the same as drawing 9 of a comparative exampleand that of drawing 10the situations shown in drawing 4 differ by forming the oblique light reflection part mentioned above as greatly as the situation of drawing 11 of a comparative example.
[0072]Namelyaccording to this embodimentas shown in drawing 4the reset gate wiring 21 which consists of polysilicon among lights which were going to pass the opening 24b and were originally going to enter into the reset drain 4 is passedAn oblique-incidence light component which the generating electric charge incorrect-mixes via the P type lateral overflow drain diffusion zone 6 to the P type charge storage field 12 (field 12 which appeared a left end in drawing 11) of the photo-diode 1 of an adjacent pixel in the case of drawing 11It is reflected on the side of the through hole 62 filled up with the side and tungsten of the oblique light reflecting film 60 which consist of an Al film of the 1st layerand enters into the P type reset drain diffusion zone 4 which should fall essentially. As a resultincorrect mixing to the P type charge storage field 12 of the photo-diode 1 of an adjacent pixel can be controlledand monitor sensitivity and monitor accuracy can be raised.
[0073]According to this embodimentas shown in drawing 4also in the portion of the photo-diode 1 similarlyThe oblique-incidence light component which passed the opening 24a in the case of drawing 11and passed the polysilicon transfer

gate wiring 20 and in which the optical generating electric charge was made to incorrect-mix to the P type reset drain diffusion 4It is reflected on the side of the through hole 61 filled up with the side and tungsten of the oblique light reflecting film 60 which were formed with the Al film of the 1st layerand enters into the P type photo-diode diffusion 12 which should fall essentially. As a resultsensitivity can be raised at the time of this photographywithout an electric charge's incorrect-mixing to the reset drain 4 at the time of a light volume monitorand reducing the light volume monitor accuracy.
[0074]About the construction material of the oblique light reflecting film 60what has the high reflectance to incident light is preferredand although metal is preferredit is preferred to consider it as the 1st layer Al film which uses aluminum as the main ingredients as well as the wiring layer of the 1st layer like this embodiment also from the compatibility of a process process. It may separate from an electrode layer or a wiring layer like this embodimentand the oblique light reflecting film 60 may be used also [wiring layer / an electrode layer or].
[0075]About the crevice between the light-shielding film 24 which is an Al film of the 2nd layerand the oblique light reflecting film 60 which is Al films of the 1st layer. Since it becomes a factor of incorrect mixing of oblique-incidence lightit is preferred to control that form the through holes 61 and 62 filled up with tungsten like this embodimentconnectand light enters into the crevice.
[0076]About the arrangement pattern of an oblique light reflection part (the oblique light reflecting film 50the through holes 61 and 62). When making it approach so that the circumference of the reset drain 4 which monitors light volume may be surrounded like this embodimentand arranging reflects an oblique-incidence light component in the position which should enter essentially effectivelyit is preferred.
[0077]If arrangement of an oblique light reflection part (the oblique light reflecting film 50the through holes 61 and 62) has asymmetry (asymmetry about point symmetry) notably to the center (namelyopening 24b) of the reset drain 4When the arrangement pattern to the reset drain 4 is made the same in all the pixelsThe dependency over the position of each pixel in the euphotic field of a solid state camera arises in the sensitivity characteristic of a light volume monitor (the light volume which is got blockedreflects by an oblique light reflection partand originally falls to the reset drain 4 by differing

according to the position of a pixel). The sensitivity characteristics of a light volume monitor differ and it is not desirable.
[0078]Namelythe optic axis of image formation lensessuch as a camerafrom being set up near the center of the field (image area) over which the pixel is distributed. While the direction to which the incident light to each pixel inclines maintains symmetry to said center (for exampleby the right-hand side pixel and a left-hand side pixel to the center of an image area.) The grade of the inclination that the direction to which incident light inclines becomes reverse becomes large toward the outside from the center (getting it blockedinclination of the light with which it enters into this as the pixel of a periphery becomes large). For this reasonif asymmetry is in a sensitivity characteristic by the element side when making the same the arrangement pattern to the reset drain 4 in all the pixelsIt is because it becomes difficult for the relation between asymmetry and a position to affect the reflection effect of the oblique-incidence light by an oblique light reflection partand to predict correctly the incident light quantity in each [within an imaging surface] position of a solid state camera.
[0079]Thereforewhen making the same the arrangement pattern of the oblique light reflection part in each pixelin each pixelit is preferred like this embodiment to arrange an oblique light reflection part to point symmetry to the center of the opening 24b. A design pattern etc. will become easy if the arrangement pattern of the oblique light reflection part in each pixel is made the same.
[0080]But as it arrangement-pattern-******** and the oblique light reflection part to the center of the opening 24b mentioned above according to the position of the pixel to the center (optic axis of an image formation lens) of image areaeven if it does not adopt arrangement of point symmetrydispersion in the sensitivity between pixels can be reduced. The example is typically shown in drawing 12. In drawing 12the mass in a grid pattern shows each pixel typically. In drawing 120 shows the optic axis (the center of image area) of the image formation lens (not shown) in space this sideand an arrow maps the direction of the incident light over a pixel at a flat surfaceand it shows it. And arrangement of the reset drain 4 and the opening 24band the oblique light reflector 60 over this is shown only about four pixels of a periphery as a representative. In this examplethe oblique light reflector 60 is arranged only to one side of the opening 24b.

[0081]By the wayabout the pixel near center Oincident light hardly inclines so that the above explanation may show. Thereforeit is not necessary to necessarily form an oblique light reflection part about the pixel near center O.
[0082][A 2nd embodiment]
[0083]Drawing 13 is an outline top view showing typically the unit pixel of the solid state camera by a 2nd embodiment of this invention. Drawing 14 is the outline sectional view which met X9-X10 line in drawing 13. Drawing 15 is the outline sectional view which met Y9-Y10 line in drawing 13. Drawing 16 is the outline sectional view which met Y11-Y12 line in drawing 13. These drawing 13 thru/or drawing 16 supports drawing 8 thru/or drawing 11 in which said comparative example is shownrespectively while it corresponds to drawing 1 thru/or drawing 4 in which said 1st embodiment is shownrespectively.
[0084]In drawing 13 thru/or drawing 16identical codes are given to an element which is the same as an element in drawing 1 thru/or drawing 4or correspondsand the overlapping explanation is omitted to it.
[0085]A place where this embodiment differs from said 1st embodimentAs the oblique light reflecting film 50 and the through holes 61 and 62 are removedinstead each pixel is shown in drawing 13drawing 14and drawing 16So that the oblique light reflecting film 70 which followed the signal read-out line (vertical signal wire) 22 which consists of an Al film of the 1st layerand one may surround the whole perimeter (namelyperimeter of the opening 24a) of the reset drain 4 for monitoring light volumeIt is the point currently formed around reset drain 4 as an oblique light reflection part. Thereforethe oblique light reflecting film 70 is used also [line / 22 / which is a wiring layer].
[0086]According to this embodimentalthough the situation of drawing 15 is the same as that of drawing 10 of a comparative examplethe situation shown in drawing 14 and drawing 16 differs from drawing 9 of a comparative example and the situation of drawing 11 which were mentioned above greatly by forming the oblique light reflecting film 70 mentioned above.
[0087]Namelythe oblique-incidence light component of the incident light which according to this embodiment passed the opening 24a as shown in drawing 14Without passing through the polysilicon reset gate 5 and making an optical generating electric charge incorrect-mix to JFET2 unlike the case of drawing 9it is reflected on the side of the oblique light reflecting film 70 formed with the Al film of the 1st layerand enters into the reset drain region 4 from

which it should fall essentially. As a resultthe sensitivity and accuracy as a light volume monitor can be raised.
[0088]According to this embodimentas shown in drawing 16the reset gate wiring 21 which consists of polysilicon among the lights which are going to pass the opening 24b and are originally going to enter into the reset drain 4 is passedThe oblique-incidence light component which the generating electric charge incorrect-mixes via the P type lateral overflow drain diffusion zone 6 to the P type charge storage field 12 (field 12 which appeared the left end in drawing 11) of the photo-diode 1 of an adjacent pixel in the case of drawing 11It is reflected on the side of the oblique light reflecting film 70 which consists of an Al film of the 1st layerand enters into the P type reset drain diffusion zone 4 which should fall essentially. As a resultincorrect mixing to the P type charge storage field 12 of the photo-diode 1 of an adjacent pixel can be controlledand monitor sensitivity and monitor accuracy can be raised.
[0089]According to this embodimentas shown in drawing 16also in the portion of the photo-diode 1 similarlyThe oblique-incidence light component which passed with the opening 24a in the case of drawing 11and passed the polysilicon transfer gate wiring 20 and in which the optical generating electric charge was made to incorrect-mix to the P type reset drain diffusion 4It is reflected on the side of the oblique light reflecting film 70 formed with the Al film of the 1st layerand enters into the P type photo-diode diffusion 12 which should fall essentially. As a resultsensitivity can be raised at the time of this photographywithout an electric charge's incorrect-mixing to a reset drain at the time of a light volume monitorand reducing the light volume monitor accuracy.
[0090]As mentioned abovealthough each embodiment of this invention was describedthis invention is not limited to these embodiments.
[0091]For examplethis invention is also applicable to various solid state camerassuch as CCDa CMOS image sensorand other amplified type image sensors. This invention is also applicable to the solid state camera which has a single light sensing portion to each pixel.
[0092]Since the oblique light reflection part which enclosed the light sensing portion on the whole or selectively is formed between the light sensing portion opening and the semiconductor substrate in the solid state camera by this inventionThe solid state camera with which

could reflect in the light sensing portion the light which entered aslant from the openingtherefore the smear was preventedand sensitivity was increased can be provided.
[0093]When the 2nd photo-diode (the 2nd light sensing portion) other than the 1st photo-diode (the 1st light sensing portion) for picturizing an object image is formed in a unit pixel as a light volume monitorThe light which entered aslant from the opening similarly can be reflected in the photo-diode which should fall essentiallyand the cross talk for these 2 pixels can be controlled.
[0094]
[Effect of the Invention]As explained aboveaccording to this inventionthe inconvenience accompanying the entering oblique light can be reduced.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is an outline top view showing typically the unit pixel of the solid state camera by a 1st embodiment of this invention.
[Drawing 2]It is the outline sectional view which met X1-X2 line in drawing 1.
[Drawing 3]It is the outline sectional view which met Y1-Y2 line in drawing 1.
[Drawing 4]It is the outline sectional view which met Y3-Y4 line in drawing 1.
[Drawing 5]It is a circuit diagram showing the equivalent circuit of the unit pixel shown in drawing 1 thru/or drawing 4.
[Drawing 6]It is a circuit diagram showing the solid state camera by a 1st embodiment of this invention.
[Drawing 7]It is a drive timing chart of a solid state camera and a shutter by a 1st embodiment of this invention.
[Drawing 8]It is an outline top view showing typically the unit pixel of the solid state camera by a comparative example.
[Drawing 9]It is the outline sectional view which met X5-X6 line in drawing 8.
[Drawing 10]It is the outline sectional view which met Y5-Y6 line in drawing 8.
[Drawing 11]It is the outline sectional view which met Y7-Y8 line in drawing 8.
[Drawing 12]It is a figure showing typically the example of the arrangement pattern of an oblique light reflection part.
[Drawing 13]It is an outline top view showing typically the

unit pixel of the solid state camera by a 2nd embodiment of this invention.
[Drawing 14]It is the outline sectional view which met X9-X10 line in drawing 13.
[Drawing 15]It is the outline sectional view which met Y9-Y10 line in drawing 13.
[Drawing 16]It is the outline sectional view which met Y11-Y12 line in drawing 13.
[Explanations of letters or numerals]
1 and 40 Photo-diode (light sensing portion)
2 JFET
3 Transfer gate
4 Reset drain
5 Reset gate
6 The lateral overflow drain diffusion zone of P type
7 Vertical scanning circuit
8 Horizontal scanning circuit
9 P channel MOS FET
10 High concentration N type silicon substrate
11 Low concentration N type epitaxial layer
12 P type photo-diode diffusion zone
13 N molding surface depletion-ized element diffusion zone
14 The N type source diffused layer of JFET
15 The P type gate diffusion layer of JFET
16 N type isolation diffusion zone
17 The N type channel diffusion layer of JFET
18 The reset drain diffusion zone of P type
20 Transfer gate wiring which consists of polysilicon
21 Reset gate wiring by polysilicon
22 Signal read-out wiring by 1st layer aluminum
24 Reset drain wiring which made the light-shielding film by the two-layer eye AL serve a double purpose
24a and 24b Opening
60 and 70 Oblique light reflecting film
61 and 62 Through hole
100 Incident light